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| Memory Products | |

82S126 82S129

1K-bit TTL bipolar PROM

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126 and 82S129 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

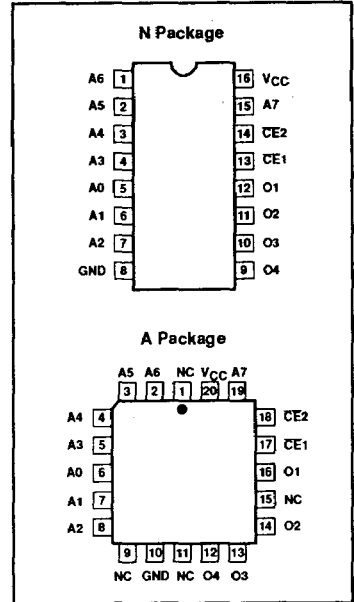
FEATURES

- Address access time: 50ns max
- Power dissipation: 0.5mW/bit typ
- Input loading: $-100\mu\text{A}$ max
- On-chip address decoding
- Two Chip Enable inputs
- Output options:
 - 82S126: Open Collector
 - 82S129: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

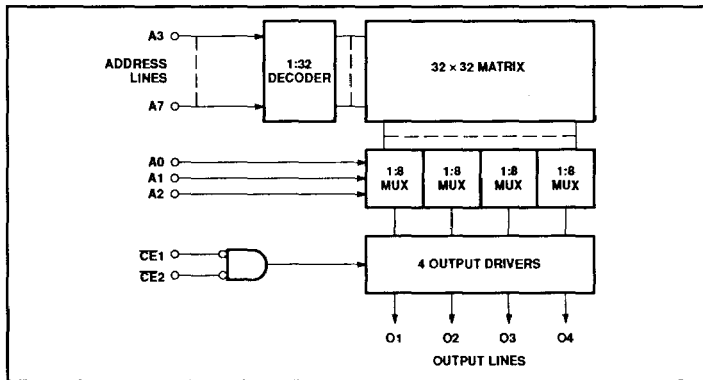
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

PIN CONFIGURATIONS



BLOCK DIAGRAM



1K-bit TTL bipolar PROM (256 × 4)

82S126 / 82S129

ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|----------------------|
| 16-Pin Plastic Dual-In-Line 300mil-wide | N82S126 N, N82S129 N |
| 20-Pin Plastic Leaded Chip Carrier 350mil-square | N82S126 A, N82S129 A |

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|-----------------------------------|-------------|-----------------|
| V _{CC} | Supply voltage | +7.0 | V _{DC} |
| V _{IN} | Input voltage | +5.5 | V _{DC} |
| V _{OH} | Output voltage High (82S126) | +5.5 | V _{DC} |
| V _O | Output voltage Off-State (82S129) | +5.5 | V _{DC} |
| T _{amb} | Operating temperature range | 0 to +75 | °C |
| T _{stg} | Storage temperature range | -65 to +150 | °C |

DC ELECTRICAL CHARACTERISTICS

0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

| SYMBOL | PARAMETER | TEST CONDITIONS ^{1,2} | LIMITS | | | UNIT |
|-----------------------------------|-------------------------------------|---|--------|------------------|------|------|
| | | | MIN | TYP ³ | MAX | |
| Input voltage | | | | | | |
| V _{IL} | Low | I _{IN} = -12mA | 2.0 | | 0.8 | V |
| V _{IH} | High | | | | | |
| V _{IC} | Clamp | | | | | |
| Output voltage | | | | | | |
| V _{OL} | Low | CE1,2 = Low I _{OUT} = 16mA | 2.4 | | 0.45 | V |
| V _{OH} | High (82S129) | I _{OUT} = -2.0mA | | | | |
| Input current | | | | | | |
| I _{IL} | Low | V _{IN} = 0.45V | | | -100 | μA |
| I _{IH} | High | V _{IN} = 5.5V | | | | |
| Output current | | | | | | |
| I _{OLK} | Leakage (82S126) | CE1 or CE2 = High, V _{OUT} = 5.5V | -15 | | 40 | μA |
| I _{OZ} | Hi-Z state (82S129) | CE1 or CE2 = High, V _{OUT} = 5.5V | | | | |
| I _{OS} | Short circuit (82S129) ⁴ | CE1 or CE2 = High, V _{OUT} = 0.5V | | | | |
| Supply current⁵ | | | | | | |
| I _{CC} | | V _{CC} = 5.25V | | | 120 | mA |
| Capacitance | | | | | | |
| C _{IN} | Input | CE1 or CE2 = High, V _{CC} = 5.0V V _{IN} = 2.0V | | 5 | | pF |
| C _{OUT} | Output | V _{OUT} = 2.0V | | 8 | | pF |

NOTES:

- Positive current is defined as into the terminal referenced.
- All voltages with respect to network ground.
- Typical values are at V_{CC} = 5V, T_{amb} = +25°C.
- Duration of short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

1K-bit TTL bipolar PROM (256 × 4)

82S126 / 82S129

AC ELECTRICAL CHARACTERISTICS

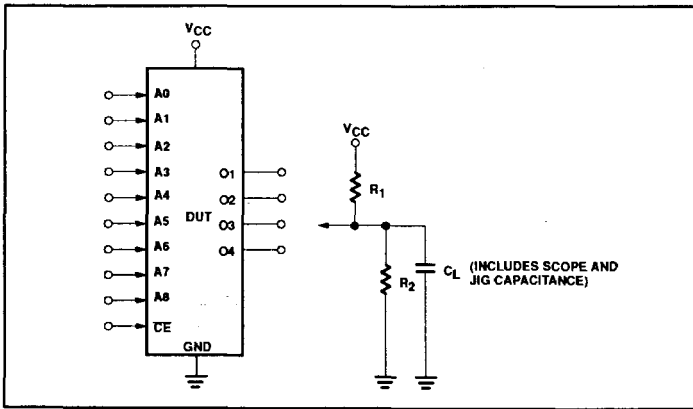
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

| SYMBOL | PARAMETER | TO | FROM | LIMITS | | | UNIT |
|---------------------------------|-----------|--------|--------------|--------|------------------|-----|------|
| | | | | MIN | TYP ¹ | MAX | |
| Access time² | | | | | | | |
| t_{AA} | | Output | Address | | 40 | 50 | ns |
| t_{CE} | | Output | Chip Enable | | | 25 | ns |
| Disable time³ | | | | | | | |
| t_{CD} | | Output | Chip Disable | | | 25 | ns |

NOTES:

1. Typical values are at $V_{\text{CC}} = 5\text{V}$, $T_{\text{amb}} = +25^\circ\text{C}$.
2. Tested at an address cycle time of $1\mu\text{s}$.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS

