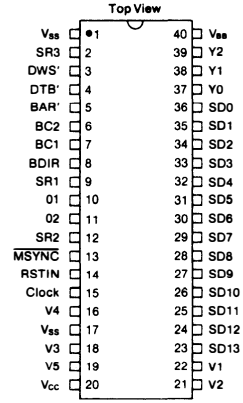
Standard Television Interface Chip

FEATURES

- Outputs include coded signal timings for CCIR or NTSC compatible video signal generation. AY-3-8900 for CCIR, AY-3-8900-1 for NTSC
- Operation from a 4.000MHz clock for AY-3-8900 and from a 3.579545MHz clock for AY-3-8900-1
- 8 coordinate addressable foreground objects on a grid of 168H by 104V for AY-3-8900 or 167H by 105V for AY-3-8900-1 of which 159 x 96 are visible positions
- Foreground objects independently programable for half height, y zoom, x zoom and 8 or 16 character lines high
- Selectable background display on a matrix of 20H x 12V using 8 x 8 picture elements
- Capable of accepting data, address and graphics information on common multiplexed bus
- 16 digitally selectable colors

PIN CONFIGURATION
40 LEAD DUAL IN LINE
AY-3-8900/AY-3-8900-1



DESCRIPTION

The AY-3-8900/8900-1 STIC is designed for use within a computer system having an external CPU and an area of ROM and RAM memory. Some of the memory must be dedicated to the support of the graphic character descriptors and patterns.

The display facilities of the circuit are separated into two simultaneously operating modes. The main chip function provides eight coordinate positioned "foreground" objects, which have a number of display options including selection from a choice of sixteen colors. The second mode provides a background display facility, which is composed of a matrix of twelve rows by twenty columns of which 19 are composed of 8 x 8 picture elements and the 20th 7 x 8 picture elements. The "background" mode utilizes a dedicated area of external memory (240 by 14 bit words) to store the character control codes for each display position and both modes require some external memory assigned to the storage of the character patterns. The graphic pattern memory is eight bits wide.

The AY-3-8900/8900-1 operates within the computer system by time sharing a bidirectional 14 bit bus. The demultiplexing and the system synchronization are defined by three sets of control signals.

The main synchronization which operates at the T.V. frame rate uses SR1, SR2 and SR3. The SR1 signal occurs once per frame and it is used to synchronize the CPU algorithms to the intended display sequences. SR1 indicates that STIC time is complete and that the AY-3-8900-1 has switched to the CPU controlled mode. SR2 is issued thirteen or fourteen times per picture frame depending on picture offset. The AY-3-8900/8900-1 takes this signal low to request the first line access for a new row of twenty characters.

The SR3 signal operates in conjunction with SR2 to read the "background" character descriptors out of external memory. The AY-3-8900/8900-1 pulses SR3 positive for each character position. Once the first line has been accessed by the SR2, SR3 combination, the following fifteen lines to complete the 8 x 8 array are fetched by SR3 alone.

The SR3 signal is also issued during the CPU controlled mode in response to BAR, ADAR or DW to enable an external device onto the 14 bit BUS.

The second control bus is used to specify address, read and write sequences for the area of external memory used to store the graphic character "dot" patterns. The three signals on this BUS are BAR', DTB' and DWS'. The BAR" is output by the AY-3-8900/8900-1 when a valid graphics character address is on the 14 bit BUS. The external memory must latch this address for future read or write operations. The DTB' signal indicates that a "read" is requested and the external memory must place the eight bits of character pattern onto the 14 bit BUS. The DWS' signal indicates that a "write" is requested.

The graphics control BUS is used during "STIC" time in the fetch of "foreground" object patterns and "background" object patterns. During the non "STIC" time when in the CPU controlled mode, the graphics control BUS can be used to link the memory area containing the graphics patterns to the main memory area of the external microprocessor.

The third control BUS communicates with the external CPU. This BUS comprises signals BC1, BC2 and BDIR. They are coded to signify address, read and write sequences. The CPU control BUS is only validated if the AY-3-8900/8900-1 is in the CPU controlled mode, otherwise it is ignored.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0° C to +40° C
Storage Temperature ..... −55° C to +150° C
All Input or Output Voltages with Respect to V_{BB} ..... −0.2V to +9.0V
V_{CC}, V_{DD} & V_{SS} with Respect to V_{BB} ..... −0.2V to +9.0V

Standard Conditions (unless otherwise noted)

T_A = 0° C to +40° C, V_{BB} = −3.3V,
V_{CC} = ±4.85V—±5.15V, V_{SS} = 0.0V

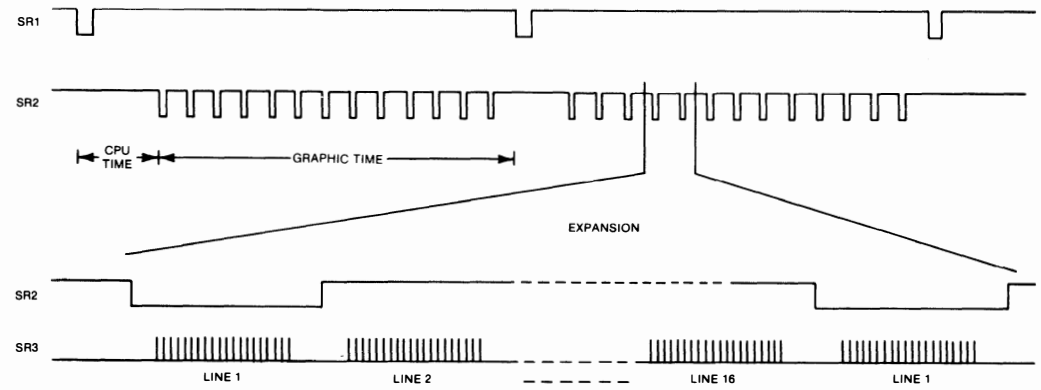
*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

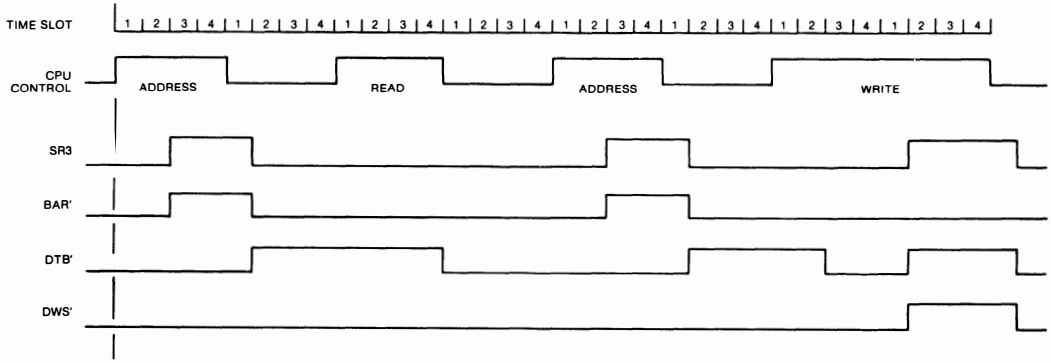
Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Bus Inputs						
Input Logic Low	V_{IL}	0	—	0.7	V	
Input Logic High	V_{IH}	2.4	—	—	V	
Input Current	I_{IL}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Outputs						
Output Logic Low	V_{OL}	0	—	0.5	V	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	V	+100pF
Supply Current						
V_{CC} Supply	I_{CC}	—	—	200	mA	V_{CC} = +5.25V @40° C
AC CHARACTERISTICS						
Clock Input Frequency	f_{cl}	—	—	—	MHz	4.000 for AY-3-8900 3.579545 for AY-3-8900-1 both externally adjusted
Bus Inputs						
Address Set Up	t_{as}	200	—	—	ns	
Address Overlap	t_{ao}	30	—	—	ns	
Write Set Up	t_{ws}	100	—	—	ns	
Write Overlap	t_{wo}	30	—	—	ns	
Bus Outputs						
Turn ON Delay	t_{da}	—	—	140	ns	1 TTL Load
Turn OFF Delay	t_{do}	0	—	—	ns	+100pF

VIDEO

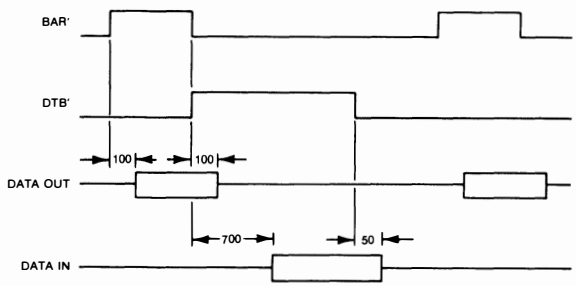
SYSTEM SYNCHRONIZATION TIMING



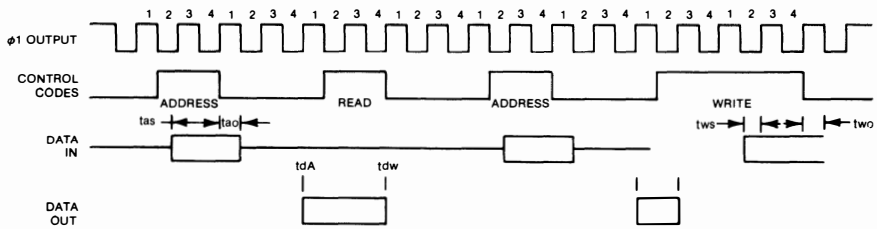
CONTROL SIGNAL OPERATION DURING CPU TIME



OBJECT FETCH TIMING



AY-3-8900-1 CPU CONTROL TIMING



VIDEO