

# 16-Bit Microprocessor

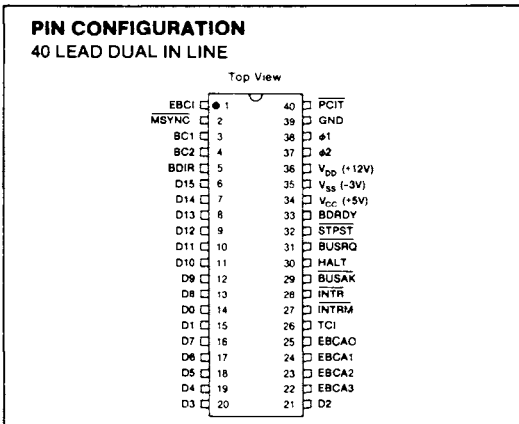
## FEATURES

- 8 program accessible 16-bit general purpose registers
- 86 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit logic and 2's complement arithmetic
- Status logic and word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- CP1610: 1μs cycle time, 2MHz 2-phase clock

## DESCRIPTION

The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with the General Instrument N-Channel Ion-Implant process, insuring high performance with proven reliability and production history. All members of the Series 1600 family are fully compatible with the CP1610.

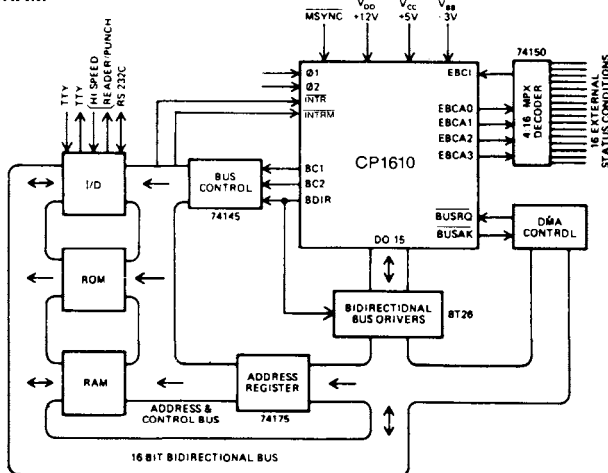
The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programable TV games, home computer systems/home information centers, programable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications. The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard,



cassette tape, floppy disk, and RS-232C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of the program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set, provides an efficient solution to micro-computer and many minicomputer-based product requirements.

## CP1610 SYSTEM DIAGRAM



## PROCESSOR SIGNALS

## DATA BUS

## D0-D15

Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

## PROCESSOR CONTROL

## STPST

Input

SToP-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

## HALT

Output

HALT: indicates that the microprocessor is in a stopped mode.

## MSYNC

Input

Master SYNC: Active low input synchronizes the microprocessor to the  $\phi 1$ ,  $\phi 2$  clocks during power-up initialization.

## EBCA 0-3

Outputs

External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXternal) instruction.

## EBCI

Input

External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

## BUS CONTROL

## BDIR, BC1, BC2

Outputs

Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

## BUSRQ

Input

## BUSAK

Output

BUS ReQuest, BUS AcKnowledge: BUSRQ\* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK\* informs devices that the bus has been released.

## BDRDY

Input

Bus Data ReaDY: causes the microprocessor to "wait" and re-synchronize to slow memory and peripheral devices.

## INTR , INTRM

INTeRrupt, INTeRrupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

## TCI

Output

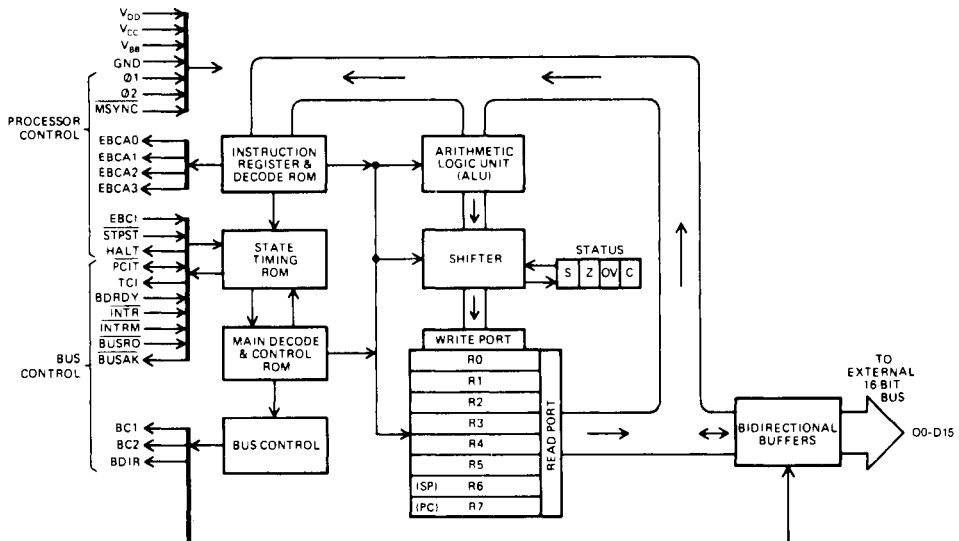
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.

## PCIT

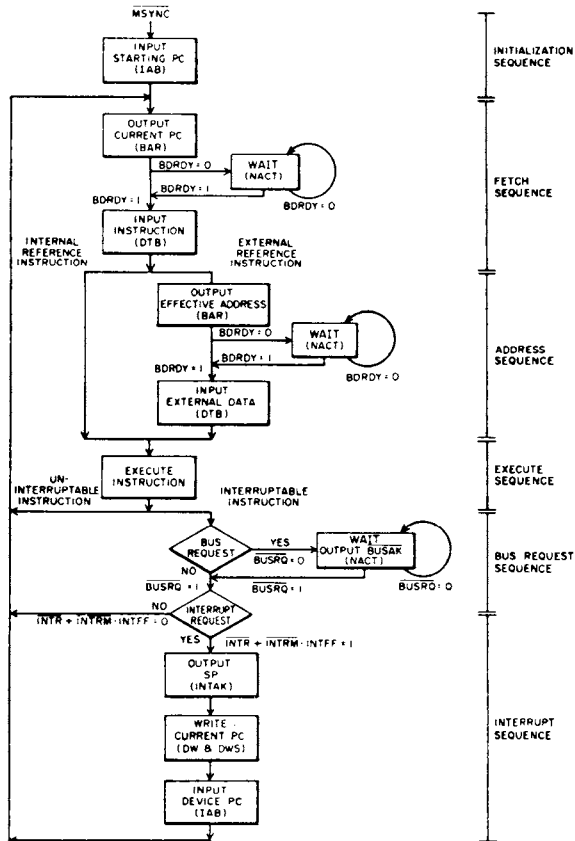
Input/output

Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INteRrupt (SIN) instruction.

CP1610 INTERNAL BLOCK DIAGRAM



**SIMPLIFIED STATE FLOW DIAGRAM**



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**BUS CONTROL SIGNALS**

BDIR	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTION, D0-D15 = high impedance
0	0	1	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	0	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	1	DTB	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	Data Write
1	1	0	DWS	Data Write Strobe
1	1	1	INTAK	INTerrupt AcKnowledge

INSTRUCTION SET (SUMMARY LISTING)

		Mnemonics	Operation	Microcycles	Comments			
INTERNAL REFERENCE INSTRUCTIONS	Register to Register	MOVR	MOVE Register	6/7	MOVR to itself MOVR to PC			
		TSTR	TeST Register	6/7				
		JR	Jump to address in Register	7	Results not stored			
		ADDR	ADD contents of Registers	6				
		SUBR	SUBtract contents of Registers	6				
		CMPR	CoMPare Registers by subtr.	6				
		ANDR	logical AND Registers	6				
	XORR	eXclusive OR Registers	6	XORR with itself				
	CLRR	CLear Register	6					
	Single Register	INCR	INCRement Register	6	One's Complement			
		DECR	DECRe ment Register	6				
		COMR	COMplement Register	6	Two's Complement			
		NEGR	NEGate Register	6				
		ADCR	ADD Carry Bit to Register	6	Pulse to $\overline{\text{PCIT}}$ pin			
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				
		SIN	Software INterrupt	6				
	RSWD	Return Status WorD	6					
	Register Shift	SWAP	SWAP 8-bit bytes	6		Add two cycles for 2-position shift.	Not interruptable. One or two position shift capability. Two position SWAP not supported.	
		SLL	Shift Logical Left	6				
RLC		Rotate Left thru Carry	6					
SLLC		Shift Logical Left thru Carry	6					
SLR		Shift Logical Right	6					
SAR		Shift Arithmetic Right	6					
RRC		Rotate Right thru Carry	6					
SARC		Shift Arithmetic Right thru Carry	6					
Control Instructions	HLT	HaLT	4	Must precede external reference to double byte data				
	SDBD	Set Double Byte Data	4					
	EIS	Enable Interrupt System	4	Not interruptable				
	DIS	Disable Interrupt System	4					
	TCI	Terminate Current Interrupt	4					
	CLRC	CLear Carry to zero	4					
SETC	SET Carry to one	4						
Jump Instructions	J	Jump	12	Return Address saved in R4, 5 or 6.				
	JE	Jump Enable interrupt	12					
	JD	Jump Disable interrupt	12					
	JSR	Jump Save Return	12					
	JSRE	Jump Save Return & Enable	12					
	JSRD	Jump Save Return & Disable interrupt	12					
EXTERNAL REFERENCE INSTRUCTIONS	Conditional Branch Instructions	B	unconditional Branch	9*	Displacement in PC+1 PC--PC±Displacement			
		NOPP	No OPeration	7*				
		BC (BLGE)	Branch on Carry	7				
		BNC (BLLT)	Branch on No Carry	7				
		BOV	Branch on OVerflow	7				
		BNOV	Branch on No OVerflow	7				
		BPL	Branch on PLUS	7				
		BMI	Branch on Minus	7				
		BZE (BEQ)	Branch on ZERo or EQual	7				
		BNZE (BNEQ)	Branch if Not ZERo or Not EQual	7				
		BLT	Branch if Less Than	7				
		BGE	Branch if Greater than or Equal	7				
		BLE	Branch if Less than or Equal	7				
		BGT	Branch if Greater Than	7				
		BUSC	Branch if Sign ≠ Carry	7				
	BESC	Branch if Sign = Carry	7					
BEXT	Branch if External condition is True	7						
				Dir.	Imm.	Indir.	Stack	
I/O	MVO	MoVe Out	11	9	9	9	Not interruptable	
	PSHR	PuSH Register to stack	—	—	—	9	PSHR=MVO@R6. Not interruptable	
	MVI	MoVe In	—	8	8	11		
	PULR	PULI from stack to Register	—	—	—	11	PULR=MVI@R6.	
Arithmetic & Logic	ADD	ADD	10	8	8	11	Result not saved	
	SUB	SUBtract	10	8	8	11		
	CMP	CoMPare	10	8	8	11		
	AND	logical AND	10	8	8	11		
	XOR	eXclusive OR	10	8	8	11		

1 MICROCYCLE=2 CLOCK CYCLES

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## ELECTRICAL CHARACTERISTICS

## Maximum Ratings\*

$V_{DD}$ , $V_{CC}$ , GND and all other Input/Output Voltages with Respect to $V_{BB}$ .....	-0.3V to +18.0V
Storage Temperature .....	-55°C to +150°C
Operating Temperature .....	0°C to +70°C

\* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

## Standard Conditions: (unless otherwise noted)

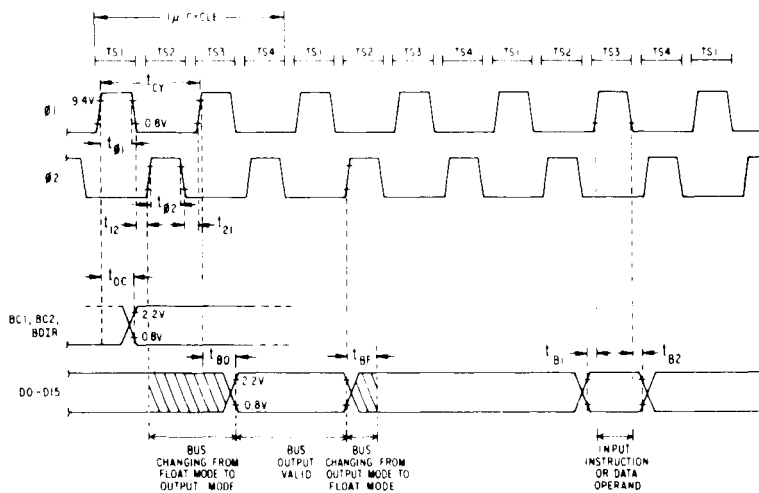
$V_{DD}$ = +11V ± 5%, 70mA (typ), 110mA (max.)	$V_{BB}$ = -2.2V ± 5%, 0.2mA (typ), 2mA (max.)
$V_{CC}$ = +5V ± 5%, 12mA (typ), 25mA (max.)	Operating Temperature ( $T_A$ ) = 0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions	
<b>DC CHARACTERISTICS</b>							
<b>Clock Inputs</b>							
High	$V_{IH}$	10	—	$V_{DD}$	V	$V_{IH} = (V_{DD} - 1)V$	
Low	$V_{IL}$	0	—	0.6	V		
Input current	$I_C$	—	—	15	mA		
<b>Logic Inputs</b>							
Low	$V_{II}$	0	—	0.65	V		
High (All Lines except BDRDY)	$V_{IH}$	2.4	—	$V_{IL}$	V		
High (Bus Data Ready Line See Note)	$V_{IHB}$	3	—	$V_{IL}$	V		
<b>Logic Outputs</b>							
High	$V_{OH}$	2.4	$V_{IL}$	—	V	$I_{OH} = 100\mu A$	
Low (Data Bus Lines D0-D15)	$V_{OL}$	—	—	0.5	V	$I_{OL} = 1.6mA$	
Low (Bus Control Lines, BC1, BC2, BDIR)	$V_{OI}$	—	—	0.45	V	$I_{OI} = 2.0mA$	
Low (All Others)	$V_{OI}$	—	—	0.45	V	$I_{OI} = 1.6mA$	
<b>AC CHARACTERISTICS</b>							
<b>Clock Pulse Inputs, <math>\phi 1</math> or <math>\phi 2</math></b>							
Pulse Width	$t_{\phi 2}, t_{\phi 1}$	250	—	—	ns	1 TTL Load & 100pF ↓	
Skew ( $\phi 1, \phi 2$ delay)	$t_{12}, t_{21}$	0	—	—	ns		
Clock Period	$t_{CY}$	0.5	—	2	$\mu s$		
Rise & Fall Times	$t_r, t_f$	—	—	15	ns		
<b>Master SYNC:</b>							
Delay from $\phi$	$t_{ms}$	—	—	30	ns		
<b>D0-D15 Bus Signals</b>							
Output delay from $\phi 1$ (float to output)	$t_{BO}$	—	—	100	ns		
Output delay from $\phi 2$ (output to float)	$t_{BF}$	—	50	—	ns		
Input setup time before $\phi 1$	$t_{B1}$	0	—	—	ns		
Input hold time after $\phi 1$	$t_{B2}$	10	—	—	ns		
<b>Bus Control Signals</b>							
<b>BC1, BC2, BDIR</b>							
Output delay from $\phi 1$	$t_{DC}$	—	—	100	ns		
Skew	—	—	—	30	ns		
BUSAK Output delay from $\phi 1$	$t_{BU}$	—	150	—	ns		
TCI Output delay from $\phi 1$	$t_{TO}$	—	200	—	ns		
TCI Pulse Width	$t_{TW}$	—	300	—	ns		
EBCA output delay from BEXT input	$t_{DE}$	—	—	150	ns		
EBCA wait time for EBCL input	$t_{AI}$	—	—	400	ns		
<b>CAPACITANCE</b>							
$\phi 1, \phi 2$ Clock Input capacitance	$C_{\phi 1}, C_{\phi 2}$	—	20	30	pF	$T_A = +25^\circ C; V_{DD} = +12V; V_{CC} = +5V;$ $V_{BB} = -3V; t_{\phi 1} = t_{\phi 2} = 120ns$	
D0-D15	—	—	8	15	pF		
All Other	—	—	5	10	pF		

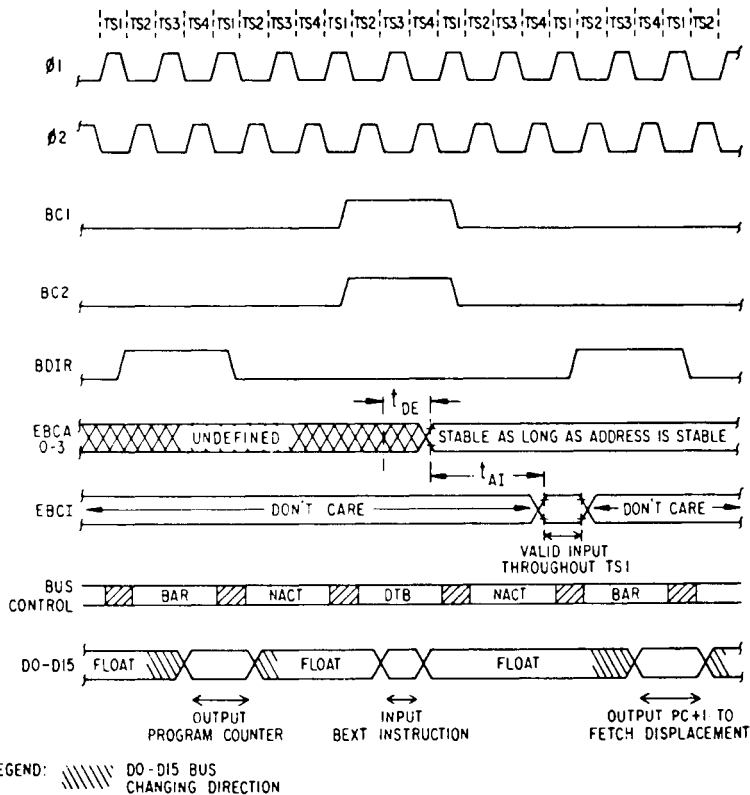
\*\*Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data Ready (BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TSI and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40  $\mu s$  duration.

CLOCK AND BUS TIMING



TYPICAL INSTRUCTION SEQUENCE (EXTERNAL BRANCH TIMING)



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